

Notice of Allowability	Application No.	Applicant(s)	
	09/588,619	DALLY ET AL.	
	Examiner	Art Unit	
	Toan D Nguyen	2665	
	Tour B rigayeri	2000	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to <u>9/10/04</u> .			
2. The allowed claim(s) is/are <u>3-22, 24-27, 29-31, 36-60, 62-64, 69 are renumbered 1-56, respectively.</u>			
3. The drawings filed on 30 January 2004 are accepted by the Examiner.			
 4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) ☐ All b) ☐ Some* c) ☐ None of the: 			
 Certified copies of the priority documents have been received. 			
2. Certified copies of the priority documents have been received in Application No			
3. Copies of the certified copies of the priority documents have been received in this national stage application from the			
International Bureau (PCT Rule 17.2(a)).			
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.			
5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.			
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.			
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached			
1) hereto or 2) to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date			
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).			
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.			
Attachment(s)	5 		4==>
 Notice of References Cited (PTO-892) Notice of Draftperson's Patent Drawing Review (PTO-948) 	5. Notice of Informal Pa	• • • • • • • • • • • • • • • • • • • •	-152)
2. In Notice of Draitperson's Patent Drawing Review (P10-946)	6. ☐ Interview Summary (Paper No./Mail Date		
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date	8), 7. Examiner's Amendm		
4. Examiner's Comment Regarding Requirement for Deposit	8. 🛛 Examiner's Stateme	nt of Reasons for Allov	vance
of Biological Material	9. Other		

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DETAILED ACTION

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

Regarding claim 6, the prior art fails to teach a combination of the steps of:

a random access memory (RAM) for storing the tree structure, an address register which stores an address to access from the RAM a scheduling value to be compared, a compare register which stores a scheduling value to be compared to the scheduling value from the RAM and a comparator for comparing the scheduling values, in the specific combination as recited in the claim.

Regarding claim 10, the prior art fails to teach a combination of the steps of:

a random access memory partitioned across pipeline stages, each pipeline stage comparing scheduling values indicated by separate portions of the tree structure and each partition storing at least one level of the tree structure; and

an address register in each pipeline stage which stores an address to access from the RAM a scheduling value to be compared, a compare register which stores a scheduling value to be compared to a scheduling value from the RAM and a comparator for comparing the scheduling values, in the specific combination as recited in the claim.

Regarding claim 12, the prior art fails to teach a combination of the steps of:

a random access memory which stores leaf nodes, a flip-flop array which identifies the winner at each internal node and a comparator for comparing scheduling values of the leaf nodes from the RAM indicated by the data stored in the flip-flop array, in the specific combination as recited in the claim.

Regarding claim 16, the prior art fails to teach a combination of the steps of: scheduling values associated with the queues, the scheduling values including scheduled transmission times according to a constant-bit-rate (CBR) guarantee wherein the scheduling values are updated to reflect byte stuffing applied to a prior packet, in the specific combination as recited in the claim.

Regarding claim 19, the prior art fails to teach a combination of the steps of: scheduling values associated with the queues, the scheduling values including scheduled transmission times according to a constant-bit-rate (CBR) guarantee and representing theoretical transmission times using a weighted-fair-queuing (WFQ) scheduling policy wherein the scheduling values are updated to reflect byte stuffing applied to a prior packet, in the specific combination as recited in the claim.

Regarding claim 25, the prior art fails to teach a combination of the steps of:
second scheduling values corresponding to a second scheduling method
associated with a second subset of queues, at least one queue being a member of each
of the first subset and second subset of queues; and

a queue selector by which first scheduling values are compared and second scheduling values are compared to select packets to be forwarded, in the specific combination as recited in the claim.

Regarding claim 29, the prior art fails to teach a combination of the steps of:
scheduling values associated with the queues, the scheduling values are being
updated to reflect byte stuffing applied to a prior packet, in the specific combination as
recited in the claim.

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Regarding claim 31, the prior art fails to teach a combination of the steps of: wherein the scheduler selects a queue by;

identifying an earliest scheduled CBR queue;

if the scheduling value of the identified CBR queue is less than or equal to a current time, transmitting a corresponding packet from the CBR queue and updating the CBR scheduling value associated with the queue; and

otherwise, transmitting a packet from a WFQ packet having an earliest scheduling value and updating the scheduling value of that queue, in the specific combination as recited in the claim.

Regarding claim 39, the prior art fails to teach a combination of the steps of:

comparing scheduling values in a selection network to select queues from which packets are forward, the selection network being a tree structure where each leaf of the tree structure represents a scheduling value of a queue and internal nodes of the tree structure represent winners in comparisons of scheduling values of sibling nodes of the tree structure wherein the tree structure is stored in a random access memory (RAM) and scheduling values from a compare register and from the RAM are compared, in the specific combination as recited in the claim.

Regarding claim 49, the prior art fails to teach a combination of the steps of:

updating the scheduling values to reflect byte stuffing applied to a prior packet, in
the specific combination as recited in the claim.

Regarding claim 52, the prior art fails to teach a combination of the steps of:

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updating the scheduling values to reflect byte stuffing applied to a prior packet, in the specific combination as recited in the claim.

Regarding claim 55, the prior art fails to teach a combination of the steps of:

updating the scheduling values to reflect byte stuffing applied to a prior packet, in
the specific combination as recited in the claim.

Regarding claim 58, the prior art fails to teach a combination of the steps of:
associating scheduling values corresponding to a second scheduling method
with a second subset of queues, at least one queue being a member of each of the first
subset and second subset of queues; and

comparing scheduling values to select packets to be forward, excess capacity under the first scheduling method being available for scheduling under the second scheduling method, in the specific combination as recited in the claim.

Regarding claim 62, the prior art fails to teach a combination of the steps of:

updating the scheduling values of a queue based on a variable length of a packet
in the queue to reflect byte stuffing applied to a prior packet, in the specific combination
as recited in the claim.

Regarding claim 64, the prior art fails to teach a combination of the steps of: wherein the scheduler selects a queue by:

identifying an earliest scheduled CBR queue;

if the scheduling value of the identified CBR queue is less than or equal to a current time, transmitting a corresponding packet from the CBR queue and updating the CBR scheduling value associated with the queue; and

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otherwise, transmitting a packet from a WFQ packet having an earliest scheduling value and updating the scheduling value of that queue, in the specific combination as recited in the claim.

Regarding claim 69, the prior art fails to teach a combination of the steps of:
second scheduling values corresponding to a second scheduling method
associated with a second subset of queues, at least one queue being a member of each
of the first subset and second subset of queues; and

queue selecting means for comparing first scheduling values and second scheduling values to select packets to be forwarded, in the specific combination as recited in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Buşiness Center (EBC) at 866-217-9197 (toll-free).

ΤN

PRIMARY EXAMINER